WHAT IS CLAIMED IS:

1. A power supply circuit comprising:

a DC-DC conversion circuit including a high side transistor and a low side transistor connected in series between a power supply voltage and a reference potential and producing a direct current output voltage as a PWM controlled output? which is obtained by turning "on" and "off" each of the transistors with each PWM signal; and

means for detecting a level of an intermediate node potential at a junction point of the high side transistor and the low side transistor after turning "off" the high side transistor, and turning "on" the low side transistor when the intermediate node potential becomes below or equal to a predetermined potential.

2. A power supply circuit comprising:

a DC-DC conversion circuit including a high side transistor and a low side transistor connected in series between a power supply voltage and a reference potential and producing a direct current output voltage as PWM controlled output which is obtained by turning "on" and "off" each of the transistors with each PWM signal;

means for obtaining an amount of error by comparing the output from the DC-DC conversion circuit to a predetermined reference voltage value;

means for

producing a PWM signal of which a pulse width is controlled by the amount of error;

supplying the PWM signal to each gate of the transistors in the DC-DC conversion circuit;

detecting a level of an intermediate node potential at a junction point of the high side transistor and the low side transistor after the high side transistor is turned "off"; and

means for turning "on" the low side transistor when the intermediate node potential becomes below or equal to a predetermined potential.

3. The power supply circuit according to claim 1, wherein the means for detecting outputs a signal for turning "on" the low side transistor when detecting the intermediate node potential lowered to the predetermined potential, which is sufficiently low with respect to the power supply voltage.

4. The power supply circuit according to claim 1, wherein the means for detecting receives the intermediate node potential by a (VDD/2) type logic circuit when setting the power supply voltage to VDD and the reference potential to zero, and outputs a signal for turning "on" the low side transistor when detecting the intermediate node potential lowered to a potential below or equal to (VDD/4).

5. A power supply circuit comprising:

a DC-DC conversion circuit including a high side transistor and a low side transistor connected in series between a power supply voltage and a reference potential and producing a direct current output voltage as PWM controlled output which is obtained by turning "on" and "off" each of the transistors with each PWM signal;

means for obtaining an amount of error by comparing the output from the DC-DC conversion circuit to a predetermined reference voltage value;

means for

producing a PWM signal of which a pulse width is controlled by the amount of error; and

supplying the PWM signal to each gate of the transistors in the DC-DC conversion circuit;

means for detecting a level of an intermediate node potential at a junction point of the high side transistor and the low side transistor after the high side

transistor is turned "off";

means for detecting a level of a PWM signal to be supplied to the gate of the low side transistor out of the PWM signals to be supplied to the DC-DC conversion circuit;

means for turning "on" the low side transistor when the first means for detecting detects the intermediate node potential lowered below or equal to a predetermined potential; and

means for turning "on" the high side transistor after the second means for detecting detects the level of the PWM signal to be supplied to the gate of the low side transistor lowered below or equal to a predetermined potential.

6. The power supply circuit according to claim 5, wherein the first means for detecting outputs a signal for turning "on" the low side transistor when detecting the intermediate node potential lowered to the predetermined potential which is sufficiently low with respect to the power supply voltage, and the second means for detecting outputs a signal for turning "on" the high side transistor when detecting the PWM signal to be supplied to the gate of the low side transistor lowered to the predetermined potential which is sufficiently low with respect to the power supply voltage.

7. The power supply circuit according to claim 5, wherein the first means for detecting receives the intermediate node potential at a (VDD/2) type logic circuit when setting the power supply voltage to VDD and the reference voltage to zero and outputs a signal for tuning on the low side transistor when detecting the intermediate node potential lowered to a potential below or equal to (VDD/4), and the second means for detecting receives the PWM signal to be supplied to the gate of the low side transistor at a (VDD/2) type logic circuit when setting the power supply voltage to VDD and the reference voltage to zero and outputs a signal for turning "on" the high side transistor after detecting the level of the PWM signal to

be supplied to the gate of the low side transistor lowered to a potential below or equal to (VDD/4).

8. The power supply circuit according to claim 2, further comprising a detection circuit which outputs a detection signal indicating that the intermediate node potential has exceeded the reference potential after returning from an undershoot at a level lower than the reference potential when the low side transistor is turned on during an "off"-period of the high side transistor, wherein means for further includes a function of turning "off" the low side transistor being in an on-state by controlling, based on a detection signal of the detection circuit, a pulse width of the PWM signal to be supplied to the gate of the low side transistor out of the PWM signals to be supplied to the DC-DC conversion circuit.

9. The power supply circuit according to claim 1, further comprising an error amplifier that produces an error signal by comparing the output voltage of the DC-DC conversion circuit with a reference voltage value of a reference voltage supply.

10. The power supply circuit according to claim 1, further comprising an output driver for receiving an input of the PWM signal.

11. The power supply circuit according to claim 1, further comprising a rectifier coil and a stabilizing capacitance connected in series between an intermediate node.

12. The power supply circuit according to claim 1, further comprising a diode connected between the source and drain of the low side transistor.

13. The power supply circuit according to claim 1, wherein the output

driver forms gate pulses to be supplied to the high side transistor and the low side transistor.

14. The power supply circuit according to claim 1, wherein the high side transistor and the low side transistor have a drain in common.

15. A power supply circuit comprising:

a DC-DC conversion circuit including a high side transistor and a low side transistor connected in series between a power supply voltage and a reference potential and producing a voltage as PWM controlled output which is obtained by turning "on" and "off" each of the transistors with each PWM signal; and

a PWM circuit and output driver that detects a level of an intermediate node potential at a junction point of the high side transistor and the low side transistor after turning "off" the high side transistor, and turning "on" the low side transistor when the intermediate node potential becomes below or equal to a predetermined potential.

16. The power supply circuit according to claim 15, wherein the PWM circuit and the output driver output a signal for turning "on" the low side transistor when detecting the intermediate node potential lowered to the predetermined potential which is sufficiently low with respect to the power supply voltage.

17. The power supply circuit according to claim 15, wherein the PWM circuit and output driver receive the intermediate node potential by a (VDD/2) type logic circuit when setting the power supply voltage to VDD and the reference potential to zero, and output a signal for turning "on" the low side transistor when detecting the intermediate node potential lowered to a potential below or equal to (VDD/4).

18. The power supply circuit according to claim 2, wherein the means for detecting outputs a signal for turning "on" the low side transistor when detecting the intermediate node potential lowered to the predetermined potential, which is sufficiently low with respect to the power supply voltage.

19. The power supply circuit according to claim 2, wherein the means for detecting receives the intermediate node potential by a (VDD/2) type logic circuit when setting the power supply voltage to VDD and the reference potential to zero, and outputs a signal for turning "on" the low side transistor when detecting the intermediate node potential lowered to a potential below or equal to (VDD/4).

20. The power supply circuit according to claim 5, further comprising a detection circuit which outputs a detection signal indicating that the intermediate node potential has exceeded the reference potential after returning from an undershoot at a level lower than the reference potential when the low side transistor is turned "on" during an "off"-period of the high side transistor, wherein the means for producing further includes a function of turning "off" the low side transistor being in an on-state by controlling, based on a detection signal of the detection circuit, a pulse width of the PWM signal to be supplied to the gate of the low side transistor out of the PWM signals to be supplied to the DC-DC conversion circuit.